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PTO/SB/08A (08-00)

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if Known	
		Application Number	09/844,668
		Filing Date	April 30, 2001
		First Named Inventor	THEKKATH
		Group Art Unit	2192
		Examiner Name	Pham, Chrystine
Sheet	1 of 1	Attorney Docket Number	MTEC-004/00US

OTHER – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
CP	D1.	F. Chow et al., "Engineering a RISC Compiler System," <i>IEEE COMP-CON</i> , March 1986, pp. 132-137.	
CP	D2.	M.D. Smith, "Tracing with Pixie," <i>Technical Report CSL-TR-91-497</i> , Stanford University, Computer Systems Laboratory, November 1991, pp. 1-29.	
CP	D3.	ATOM Reference Manual, <i>Digital Equipment Corporation</i> , Massachusetts, December 1993, pp. 1-32.	
CP	D4.	A. Srivastaba et al., "ATOM: A System for Building Customized Program Analysis Tools," <i>WRL, Research Report 94/2</i> , Digital Equipment Corporation, Massachusetts, March 1994, pp. 1-23.	
CP	D5.	ATOM User Manual, Digital Equipment Corporation, March 1994, pp. 1-28.	
CP	D6.	B. Cmelik et al., "Shade: A Fast Instruction-Set Simulator for Execution Profiling," <i>Proceedings of the 1994 ACM SIGMETRICS Conference</i> , SIGMETRICS, California, May 1994, pp. 128-137.	
CP	D7.	MIPS Technologies; "MIPS64 5K™ Processor Core Integrator's Guide;" [Document No. MD00056]; <i>MIPS Technologies, Inc.</i> ; Rev. 1.2; August 11, 2000; pp. I-II, 1-82.	
CP	D8.	MIPS Technologies; "MIPS64™ 5K™ Processor Core Family Integrator's Guide;" [Document No. MD00106]; <i>©1999-2001 MIPS Technologies, Inc.</i> ; Rev. 02.00; January 15, 2001; pp. I-VIII, 1-75.	
CP	D9.	MIPS Technologies; "Core Processor Interface Specification;" [Document No. MD00068]; <i>MIPS Technologies, Inc.</i> ; Rev. 1.11; March 30, 2001; pp. 1-26.	

Examiner Signature	/Chrystine Pham/	Date Considered (08/16/2006)	
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		Group Art Unit	2122
		Examiner Name	Pham, Chrystine
Sheet	1 of 1	Attorney Docket Number	MTEC-004/00US

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY
		Office ¹	Number ²	Kind Code ³ (if known)		

OTHER - NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
CP	D1	Susan J. EGGERS, et al., "Techniques for Efficient Inline Tracing on a Shared-Memory Multiprocessor," University of Washington, 1990 ACM, pp. 37-47.		
CP	D2	Richard A. UHLIG, et al., "Trace-Driven Memory Simulation: A Survey," Intel Microcomputer Research Lab; University of Michigan, ACM Computing Surveys, Vol. 29, No. 2, June 1997, pp. 128-170.		
CP	D3	Eric ROTENBERG, et al., "Trace Processors," University of Wisconsin, 1997 IEEE Service Center, 12 pp.		
CP	D4	E.N. ELNOZAHY, "Address Trace Compression Through Loop Detection and Reduction," ©1999 ACM 1-58113-083, pp. 214, 215.		
CP	D5	Darren JONES, "Opal Coprocessor Interface," MIP Proprietary/Confidential, June 4, 1999, pp. 1-18.		
CP	D6	Darren JONES, MIPSS64™ SKC™ Processor Cores User's Manual, Rev. 1.0, July 4, 1999, pp. 6-1 to 6-26.		
CP	D7	MIPSS64™ SKC™ Processor Cores User's Manual, Rev. 1.0.1., 1999, pp. 247-276.		

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